WE CLAIM:

1. Apparatus for processing data, said apparatus comprising:

at least one memory having a plurality of memory storage locations associated with respective memory addresses; and

a self-test controller operable to control self-test of said at least one memory; wherein

said self-test controller is responsive to a self-test instruction to perform at least one memory access to each memory location within a sequence of memory storage locations, memory address changes between successive memory locations accessed within said sequence of memory storage locations being selected in dependence upon said self-test instruction such that said self-test controller may be configured by said self-test instruction to implement different memory test methodologies.

2. Apparatus as claimed in claim 1, wherein said self-test controller is operable to execute a plurality of self-test instructions to perform a sequence of memory tests, said self-test instructions being programmable to allow different sequences of memory tests to be specified by different users.

3. Apparatus as claimed in claim 2, wherein said sequence of memory tests may be changed to match different memories.

4. Apparatus as claimed in claim 2, wherein said sequence of memory tests may be changed to match different fabrication characteristics and test needs.

5. Apparatus as claimed in claim 1, wherein said memory addresses are physical row and column addresses within said at least one memory.

6. Apparatus as claimed in claim 1, wherein said self-test instruction specifies data to be written to said memory as part of said at least one memory access.

7. Apparatus as claimed in claim 1, wherein said memory address changes between successive memory locations as selected in dependence upon said self-test instruction and said self-test controller allow one or more of the following memory test operations to be performed:

(i) write specified data to all memory locations within a range of memory addresses;

(ii) read data from all memory locations within a range of memory addresses;

(iii) write specified data to memory locations having a checkerboard pattern of memory addresses;

(iv) read data from memory locations having a checkerboard pattern of memory addresses;

(v) conduct a march C memory test;

(vi) read data from and write specified data to a sequence of memory locations within a memory arranged in rows and columns of memory locations such that memory locations within a row of memory locations are accessed in turn before a next row of memory locations is selected for access;

(vii) read data from and write specified data to a sequence of memory locations within a memory arranged in rows and columns of memory locations such that memory locations within a column of memory locations are accessed in turn before a next column of memory locations is selected for access;

(viii) read data from, write specified data to and read data from a sequence of memory locations within a memory arranged in rows and columns of memory locations such that memory locations within a row of memory locations are accessed in turn before a next row of memory locations is selected for access;

(ix) read data from, write specified data to and read data from to a sequence of memory locations within a memory arranged in rows and columns of memory

locations such that memory locations within a column of memory locations are accessed in turn before a next column of memory locations is selected for access;

(x) for a sequence of memory locations, repeatedly write a value to one or more bitlines within said memory and then read a complementary value stored within a memory location sharing said one or more bitlines; and

(xi) for a sequence of memory locations, repeatedly read a value from a memory location while interjecting opposing data writes;

(xii) a predetermined combination of memory test operations as defined in (i) to (xi) for go/nogo testing where manufacture's test methods do not have specific requirements; and

(xiii) creating false read data at specific points in order to validate fail detection.

8. Apparatus as claimed in claim 1, further comprising a processor core, said processor core, said at least one memory and said self-test controller being formed together on an integrated circuit.

9. Apparatus as claimed in claim 1, wherein said at least one memory is one of a synthesized memory and a custom memory.

10. Apparatus as claimed in claim 1, wherein an interface circuit is disposed between said self-test controller and said at least one memory, said interface circuit serving to adapted values and timings of signals passed between said self-test controller and said at least one memory to accommodate differing value and timing properties of said at least one memory.

11. Apparatus as claimed in claim 10, wherein said interface circuit maps a memory address value generated by said self-test controller to a logical address value to be input to said at least one memory.

12. Apparatus as claimed in claim 1, comprising a plurality of memories and said self-test instruction specifies to which of said plurality of memories said self-test instruction is to be applied.

13. Apparatus as claimed in claim 1, wherein said self-test instruction specifies in which of a plurality of different ways a detected memory error is to be reported by said self-test controller.

14. Apparatus as claimed in claim 10, wherein said interface circuit includes a result data register in which result data from testing said at least one memory may be captured and said self-test controller is responsive to a self-test instruction to read result data from said result data register.

15. Apparatus as claimed in claim 1, wherein said self-test instruction specifies a size of said at least one memory to be tested.

16. Apparatus as claimed in claim 1, wherein said self-test instruction is serially loaded into said self-test controller.

17. Apparatus as claimed in claim 1, wherein said at least one memory and said self-test controller are formed together on an integrated circuit having a plurality of external signal pins, said self-test controller having one or more external signal pins through which one or more self-test instructions may be applied to said self-test controller.

18. A method of testing a memory having a plurality of memory storage locations associated with respective memory addresses, said method comprising the steps of:

passing a self-test instruction to a self-test controller coupled to said memory; and

in response to said self-test instruction, performing at least one memory access to each memory location within a sequence of memory storage locations, memory address changes between successive memory locations accessed within said sequence of memory storage locations being selected in dependence upon said self-test instruction such that said self-test controller may be configured by said self-test instruction to implement different memory test methodologies.

19. A method as claimed in claim 18, comprising executing a plurality of self-test instructions with said self-test controller to perform a sequence of memory tests, said self-test instructions being programmable to allow different sequences of memory tests to be specified by different users.

20. A method as claimed in claim 19, wherein said sequence of memory tests may be changed to match different memories.

21. A method as claimed in claim 19, wherein said sequence of memory tests may be changed to match different fabrication characteristics and test needs.

22. A method as claimed in claim 18, wherein said memory addresses are physical row and column addresses within said at least one memory.

23. A method as claimed in claim 1, wherein said self-test instruction specifies data to be written to said memory as part of said at least one memory access.

24. A method as claimed in claim 1, wherein said memory address changes between successive memory locations as selected in dependence upon said self-test instruction and said self-test controller allow one or more of the following memory test operations to be performed:

(i) write specified data to all memory locations within a range of memory addresses;

(ii) read data from all memory locations within a range of memory addresses;

(iii) write specified data to memory locations having a checkerboard pattern of memory addresses;

(iv) read data from memory locations having a checkerboard pattern of memory addresses;

(v) conduct a march C memory test;

(vi) read data from and write specified data to a sequence of memory locations within a memory arranged in rows and columns of memory locations such that memory locations within a row of memory locations are accessed in turn before a next row of memory locations is selected for access;

(vii) read data from and write specified data to a sequence of memory locations within a memory arranged in rows and columns of memory locations such that memory locations within a column of memory locations are accessed in turn before a next column of memory locations is selected for access;

(viii) read data from, write specified data to and read data from a sequence of memory locations within a memory arranged in rows and columns of memory locations such that memory locations within a row of memory locations are accessed in turn before a next row of memory locations is selected for access;

(ix) read data from, write specified data to and read data from to a sequence of memory locations within a memory arranged in rows and columns of memory locations such that memory locations within a column of memory locations are accessed in turn before a next column of memory locations is selected for access;

(x) for a sequence of memory locations, repeatedly write a value to one or more bitlines within said memory and then read a complementary value stored within a memory location sharing said one or more bitlines; and

(xi) for a sequence of memory locations, repeatedly read a value from a memory location while interjecting opposing data writes;

(xii) a predetermined combination of memory test operations as defined in (i) to (xi) for go/nogo testing where manufacture's test methods do not have specific requirements; and

(xiii) creating false read data at specific points in order to validate fail detection.

25. A method as claimed in claim 18, wherein said at least one memory and said self-test controller formed together with a processor core on an integrated circuit.

26. A method as claimed in claim 18, wherein said at least one memory is one of a synthesized memory or a custom memory.

27. A method as claimed in claim 18, wherein values and timings of signals passed between said self-test controller and said at least one memory are adapted by an interface circuit disposed between said self-test controller and said at least one memory in order to accommodate differing value and timing properties of said at least one memory.

28. A method as claimed in claim 27, wherein said interface circuit maps a memory address value generated by said self-test controller to a logical address value to be input to said at least one memory.

29. A method as claimed in claim 18, wherein said self-test instruction specifies to which of a plurality of memories said self-test instruction applies.

30. A method as claimed in claim 18, wherein said self-test instruction specifies in which of a plurality of different ways a detected memory error is to be reported by said self-test controller.

31. A method as claimed in claim 27, wherein said interface circuit includes a result data register in which result data from testing said at least one memory may be captured and said self-test controller is responsive to a self-test instruction to read result data from said result data register.

32. A method as claimed in claim 18, wherein said self-test instruction specifies a size of said at least one memory to be tested.

33. A method as claimed in claim 18, wherein said self-test instruction is serially loaded into said self-test controller.

34. A method as claimed in claim 18, wherein said at least one memory and said self-test controller are formed together on an integrated circuit having a plurality of external signal pins, said self-test controller having one or more external signal pins through which one or more self-test instructions may be applied to said self-test controller.